# HD74LS259

## 8-bit Address Latch

REJ03D0471–0200
Rev.2.00
Feb.18.2005

This 8-bit addressable latch is designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. This is multifunctional device capable of storing single-line data in eight addressable latches, and being a 1-to-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear and enable inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch.

The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, latch remains in their previous states and is unaffected by the data or address inputs.

To eliminate the possibility of entering erroneous data in the latch, the enable should be held high (inactive) while the address lines are changing.

In the clear mode, all outputs are low and unaffected by the address and data inputs.



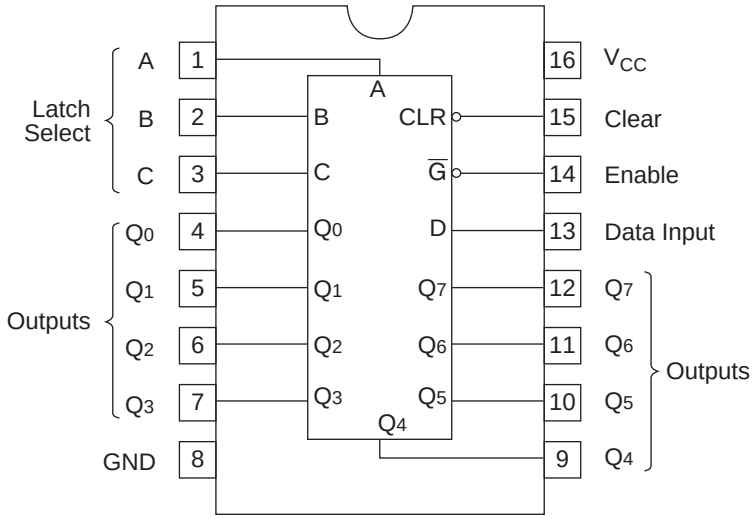
### Features

- Ordering Information

| Part Name | Package Type | Package Code (Previous Code) | Package Abbreviation | Taping Abbreviation (Quantity) |
|---|---|---|---|---|
| HD74LS259P | DILP-16 pin | PRDP0016AE-B (DP-16FV) | — | — |
| HD74LS259FPEL | SOP-16 pin (JEITA) | PRSP0016DH-B (FP-16DAV) | FP | EL (2,000 pcs/reel) |
| HD74LS259RPEL | SOP-16 pin (JEDEC) | PRSP0016DG-A (FP-16DNV) | RP | EL (2,500 pcs/reel) |

Note: Please consult the sales office for the above package availability.

## Pin Arrangement




(Top view)

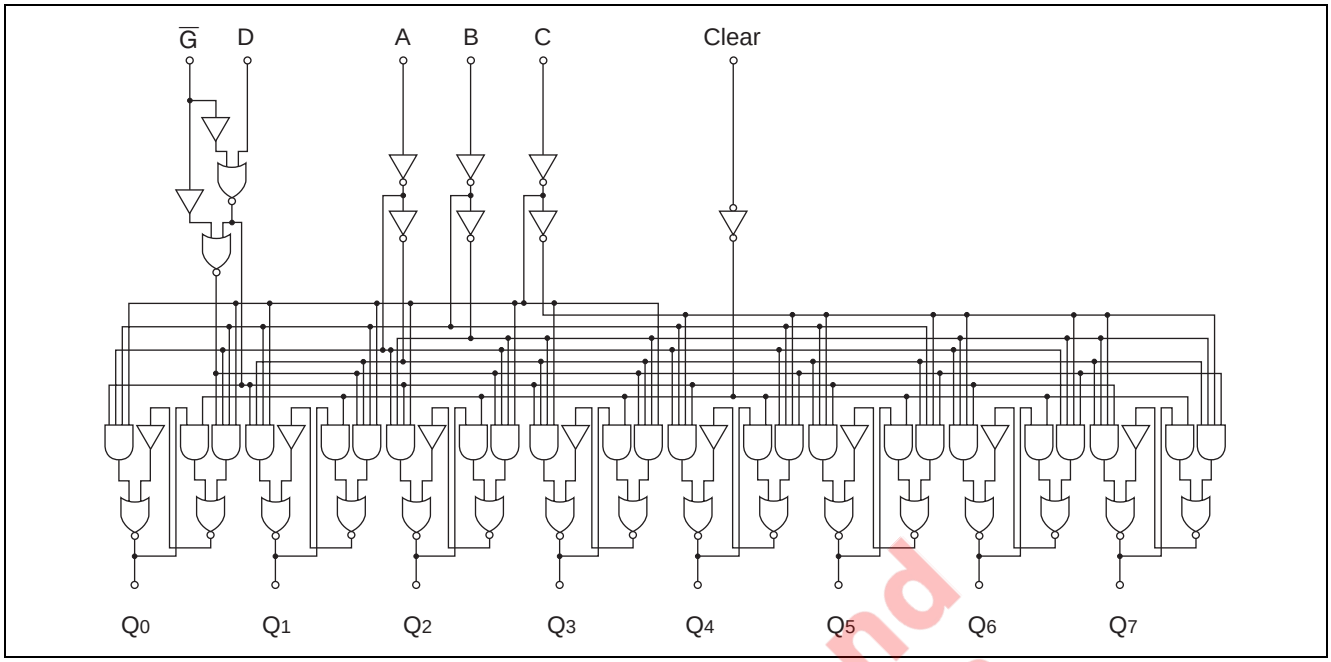
## Function Table

| Input | | Output of addressed latch | Each other output | Function |
|---|---|---|---|---|
| CLR | $\overline{G}$ | | | |
| H | L | D | Qio | Addressable latch |
| H | H | Qio | Qio | Memory |
| L | L | D | L | 8-line demultiplexer |
| L | H | L | L | Clear |

| Select inputs | | | Latch addressed |
|---|---|---|---|
| C | B | A | |
| L | L | L | 0 |
| L | L | H | 1 |
| L | H | L | 2 |
| L | H | H | 3 |
| H | L | L | 4 |
| H | L | H | 5 |
| H | H | L | 6 |
| H | H | H | 7 |

Notes: 1. H; high level, L; low level
2. D; the level at the data input
3. $O_{io}$; the level of $Q_i$ (i = 0, 1, … 7, as appropriate) before the indicated steady state input conditions were established.

## Block Diagram




## Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 7 | V |
| Input voltage | $V_{IN}$ | 7 | V |
| Power dissipation | $P_T$ | 400 | mW |
| Storage temperature | Tstg | –65 to +150 | °C |

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.



## Recommended Operating Conditions

| Item | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | | $V_{CC}$ | 4.75 | 5.00 | 5.25 | V |
| Output current | | $I_{OH}$ | — | — | –400 | µA |
| | | $I_{OL}$ | — | — | 8 | mA |
| Operating temperature | | Topr | –20 | 25 | 75 | °C |
| Pulse width | | $t_w$ | 15 | — | — | ns |
| Setup time | Data | $t_{su}$ | 20↑ | — | — | ns |
| | Address | $t_{su}$ | 20↑ | — | — | ns |
| Hold time | Data | $t_h$ | 0↑ | — | — | ns |
| | Address | $t_h$ | 0↑ | — | — | ns |

## Electrical Characteristics

(Ta = –20 to +75 °C)

| Item | Symbol | min. | typ.* | max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | 2.0 | — | — | V | |
| | $V_{IL}$ | — | — | 0.8 | V | |
| Output voltage | $V_{OH}$ | 2.7 | — | — | V | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = –400 µA |
| | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 4 mA, $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V |
| | | — | — | 0.5 | | $I_{OL}$ = 8 mA |
| Input current | $I_{IH}$ | — | | 20 | µA | $V_{CC}$ = 5.25 V, $V_I$ = 2.7 V |
| | $I_{IL}$ | — | | –0.4 | mA | $V_{CC}$ = 5.25 V, $V_I$ = 0.4 V |
| | $I_I$ | — | | 0.1 | mA | $V_{CC}$ = 5.25 V, $V_I$ = 7 V |
| Short-circuit output current | $I_{OS}$ | –20 | — | –100 | mA | $V_{CC}$ = 5.25 V |
| Supply current** | $I_{CC}$ | — | 22 | 36 | mA | $V_{CC}$ = 5.25 V |
| Input clamp voltage | $V_{IK}$ | — | — | –1.5 | V | $V_{CC}$ = 4.75 V, $I_{IN}$ = –18 mA |

Notes: * $V_{CC}$ = 5 V, Ta = 25°C

** $I_{CC}$ is measured with all outputs open and all inputs grounded.

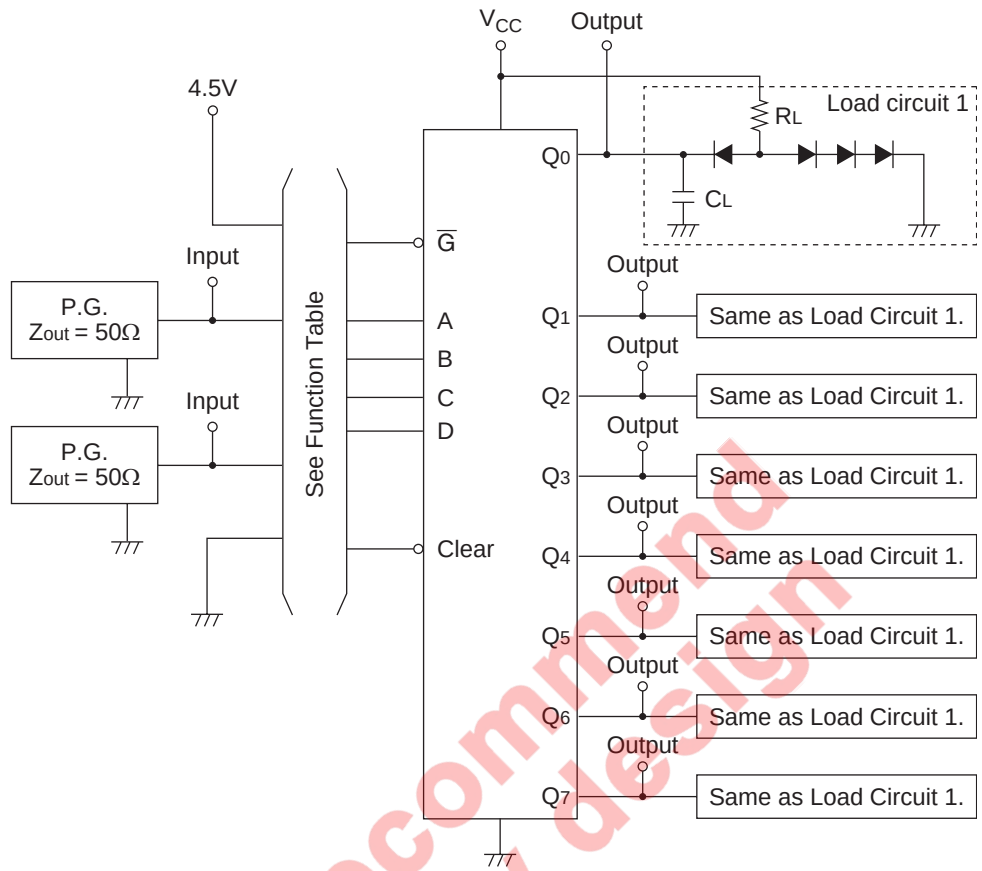
## Switching Characteristics

($V_{CC}$ = 5 V, Ta = 25°C)

| Item | Symbol | Inputs | Output | min. | typ. | max. | Unit | Condition |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PHL}$ | Clear | $Q_0$ to $Q_7$ | — | 17 | 27 | ns | $C_L$ = 15 pF, $R_L$ = 2 kΩ |
| | $t_{PLH}$ | Data | $Q_0$ to $Q_7$ | — | 20 | 32 | ns | |
| | $t_{PHL}$ | | | — | 13 | 21 | | |
| | $t_{PLH}$ | Address | $Q_0$ to $Q_7$ | — | 24 | 38 | ns | |
| | $t_{PHL}$ | | | — | 18 | 29 | | |
| | $t_{PLH}$ | Enable | $Q_0$ to $Q_7$ | — | 22 | 35 | ns | |
| | $t_{PHL}$ | | | — | 15 | 24 | | |

## Testing Method

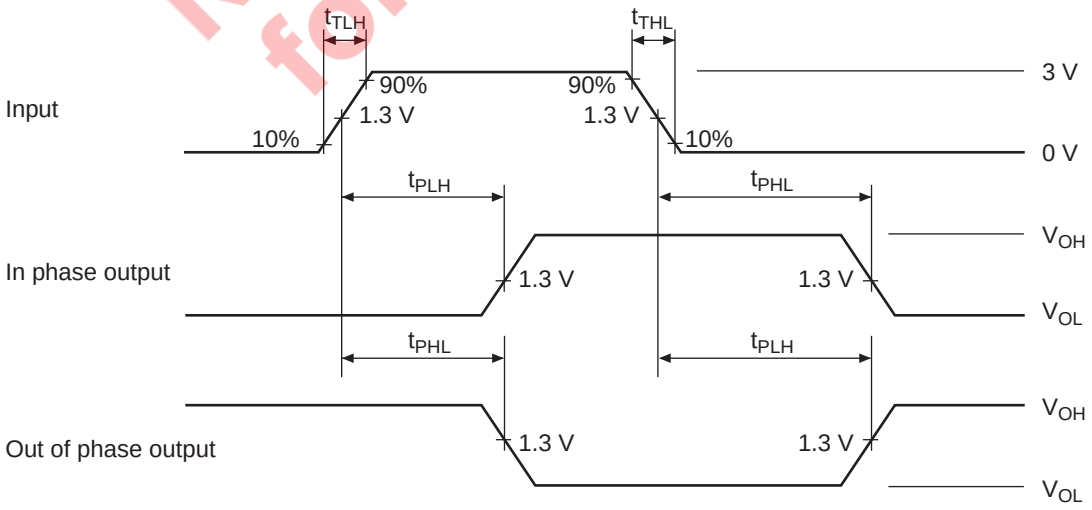
### Test Circuit




Notes: 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1S2074(H).



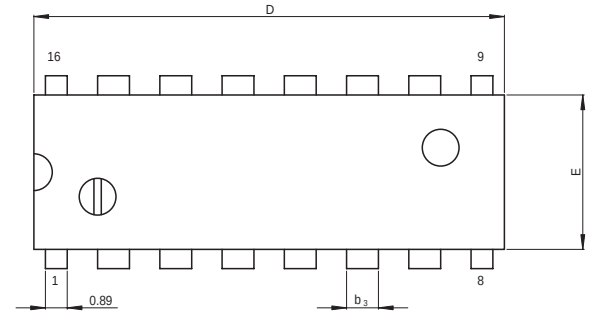
### Waveform

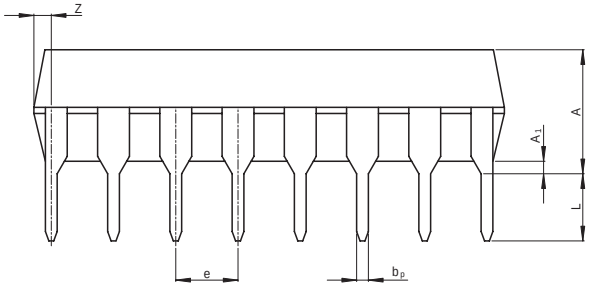


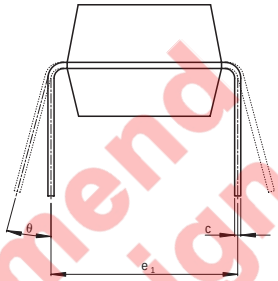

Note: Input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle 50%

## Package Dimensions

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-DIP16-6.3x19.2-2.54 | PRDP0016AE-B | DP-16FV | 1.05g |



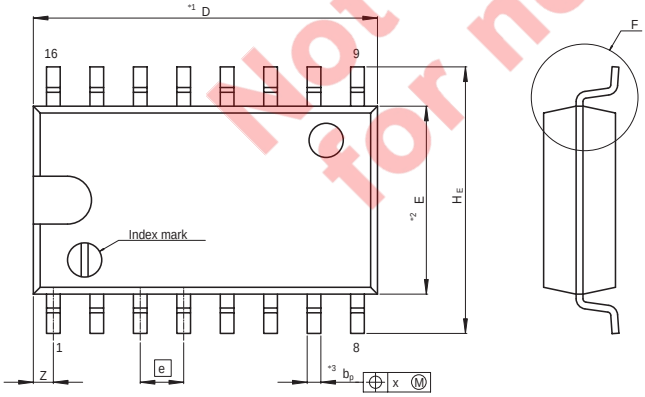



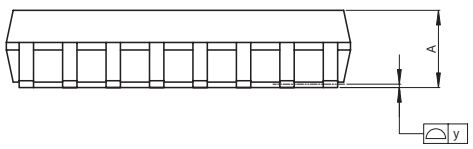

( Ni/Pd/Au plating )

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| e 1 | —— | 7.62 | —— |
| D | —— | 19.2 | 20.32 |
| E | —— | 6.3 | 7.4 |
| A | —— | —— | 5.06 |
| A 1 | 0.51 | —— | —— |
| b p | 0.40 | 0.48 | 0.56 |
| b 3 | —— | 1.30 | —— |
| c | 0.19 | 0.25 | 0.31 |
| θ | 0° | —— | 15° |
| e | 2.29 | 2.54 | 2.79 |
| Z | —— | —— | 1.12 |
| L | 2.54 | —— | —— |

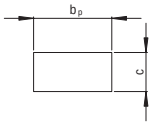


| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-SOP16-5.5x10.06-1.27 | PRSP0016DH-B | FP-16DAV | 0.24g |

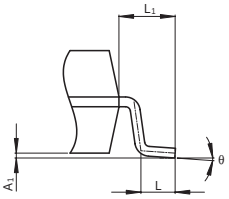



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2"
   DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT
   INCLUDE TRIM OFFSET.



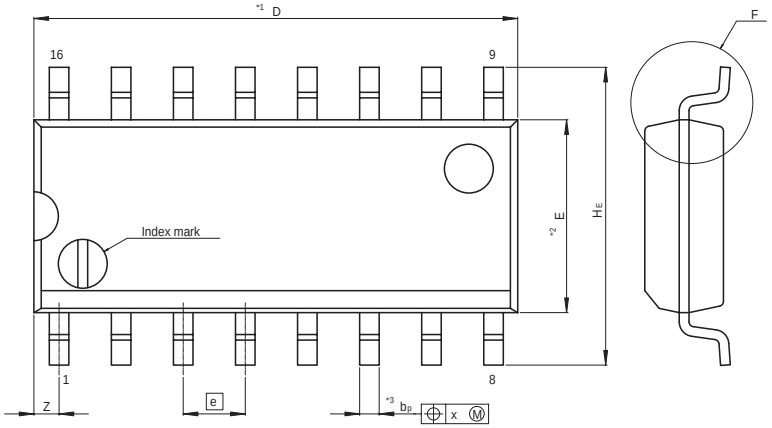

Terminal cross section
( Ni/Pd/Au plating )




Detail F

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | —— | 10.06 | 10.5 |
| E | —— | 5.50 | —— |
| A 2 | —— | —— | —— |
| A 1 | 0.00 | 0.10 | 0.20 |
| A | —— | —— | 2.20 |
| b p | 0.34 | 0.40 | 0.46 |
| b 1 | —— | —— | —— |
| c | 0.15 | 0.20 | 0.25 |
| c 1 | —— | —— | —— |
| θ | 0° | —— | 8° |
| H E | 7.50 | 7.80 | 8.00 |
| e | —— | 1.27 | —— |
| x | —— | —— | 0.12 |
| y | —— | —— | 0.15 |
| Z | —— | —— | 0.80 |
| L | 0.50 | 0.70 | 0.90 |
| L 1 | —— | 1.15 | —— |

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-SOP16-3.95x9.9-1.27 | PRSP0016DG-A | FP-16DNV | 0.15g |




NOTE)
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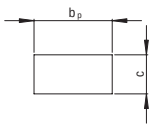
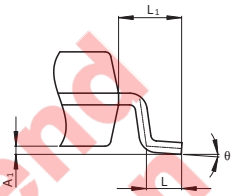
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.




Terminal cross section
( Ni/Pd/Au plating )




Detail F

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | —— | 9.90 | 10.30 |
| E | —— | 3.95 | —— |
| $A_2$ | —— | —— | —— |
| $A_1$ | 0.10 | 0.14 | 0.25 |
| A | —— | —— | 1.75 |
| $b_p$ | 0.34 | 0.40 | 0.46 |
| $b_1$ | —— | —— | —— |
| c | 0.15 | 0.20 | 0.25 |
| $c_1$ | —— | —— | —— |
| θ | 0° | —— | 8° |
| $H_E$ | 5.80 | 6.10 | 6.20 |
| e | —— | 1.27 | —— |
| x | —— | —— | 0.25 |
| y | —— | —— | 0.15 |
| Z | —— | —— | 0.635 |
| L | 0.40 | 0.60 | 1.27 |
| $L_1$ | —— | 1.08 | —— |

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