

# HD74LS259

## 8-bit Address Latch

REJ03D0471-0200

Rev.2.00

Feb.18.2005

This 8-bit addressable latch is designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. This is multifunctional device capable of storing single-line data in eight addressable latches, and being a 1-to-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear and enable inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch.

The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, latch remains in their previous states and is unaffected by the data or address inputs.

To eliminate the possibility of entering erroneous data in the latch, the enable should be held high (inactive) while the address lines are changing.

In the clear mode, all outputs are low and unaffected by the address and data inputs.

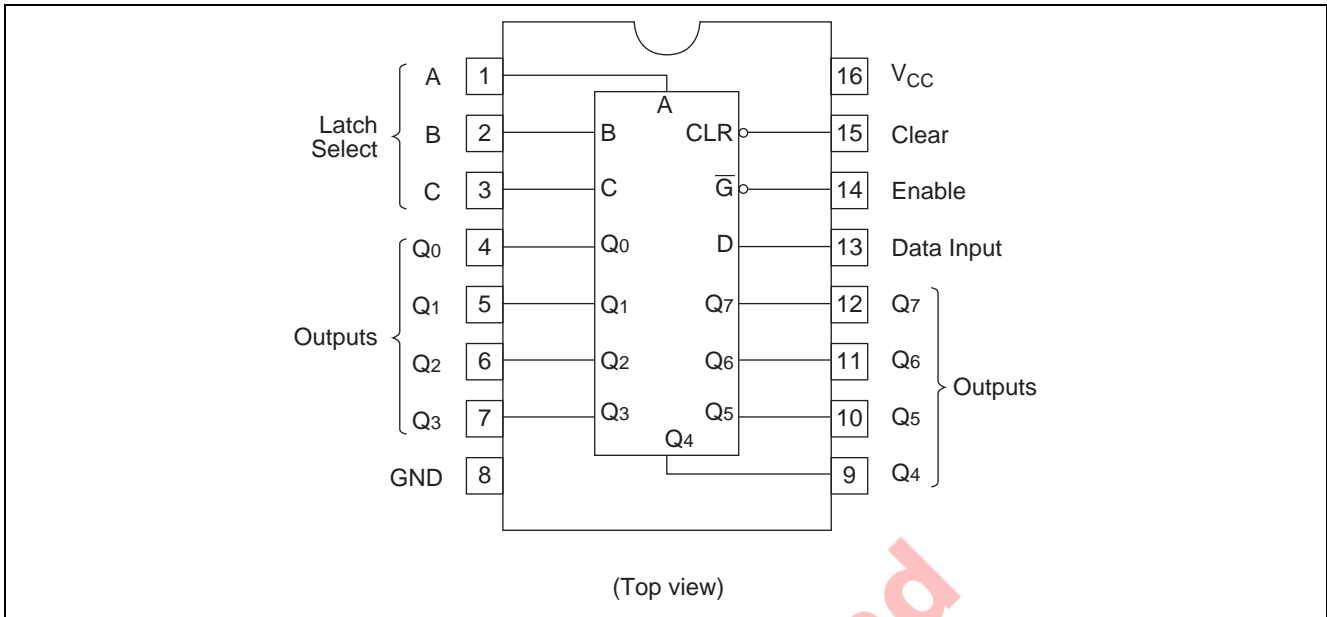
### Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS259P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	—	—
HD74LS259FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74LS259RPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



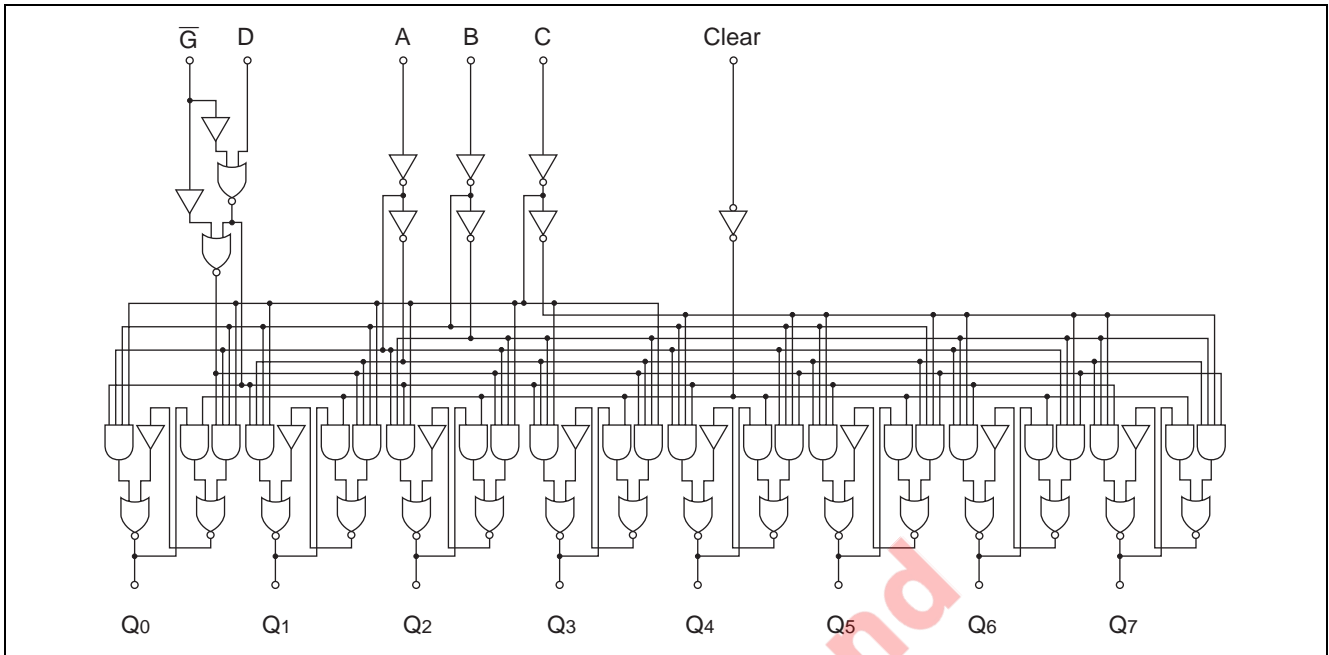
Function Table

Input		Output of addressed latch	Each other output	Function
CLR	$\bar{G}$			
H	L	D	$Q_{io}$	Addressable latch
H	H	$Q_{io}$	$Q_{io}$	Memory
L	L	D	L	8-line demultiplexer
L	H	L	L	Clear

Select inputs			Latch addressed
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

- Notes: 1. H; high level, L; low level  
 2. D; the level at the data input  
 3.  $O_{io}$ ; the level of  $Q_i$  ( $i = 0, 1, \dots, 7$ , as appropriate) before the indicated steady state input conditions were established.

**Block Diagram**



**Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit
Supply voltage	$V_{CC}$	7	V
Input voltage	$V_{IN}$	7	V
Power dissipation	$P_T$	400	mW
Storage temperature	$T_{stg}$	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

**Recommended Operating Conditions**

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.75	5.00	5.25	V
Output current	$I_{OH}$	—	—	-400	μA
	$I_{OL}$	—	—	8	mA
Operating temperature	$T_{opr}$	-20	25	75	°C
Pulse width	$t_w$	15	—	—	ns
Setup time	Data	$t_{su}$	20↑	—	ns
	Address	$t_{su}$	20↑	—	ns
Hold time	Data	$t_h$	0↑	—	ns
	Address	$t_h$	0↑	—	ns

## Electrical Characteristics

(Ta = -20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V <sub>IH</sub>	2.0	—	—	V	
	V <sub>IL</sub>	—	—	0.8	V	
Output voltage	V <sub>OH</sub>	2.7	—	—	V	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -400 μA
	V <sub>OL</sub>	—	—	0.4	V	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V
—		—	0.5			
Input current	I <sub>IH</sub>	—	—	20	μA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 2.7 V
	I <sub>IL</sub>	—	—	-0.4	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 0.4 V
	I <sub>I</sub>	—	—	0.1	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 7 V
Short-circuit output current	I <sub>OS</sub>	-20	—	-100	mA	V <sub>CC</sub> = 5.25 V
Supply current**	I <sub>CC</sub>	—	22	36	mA	V <sub>CC</sub> = 5.25 V
Input clamp voltage	V <sub>IK</sub>	—	—	-1.5	V	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA

Notes: \* V<sub>CC</sub> = 5 V, Ta = 25°C\*\* I<sub>CC</sub> is measured with all outputs open and all inputs grounded.

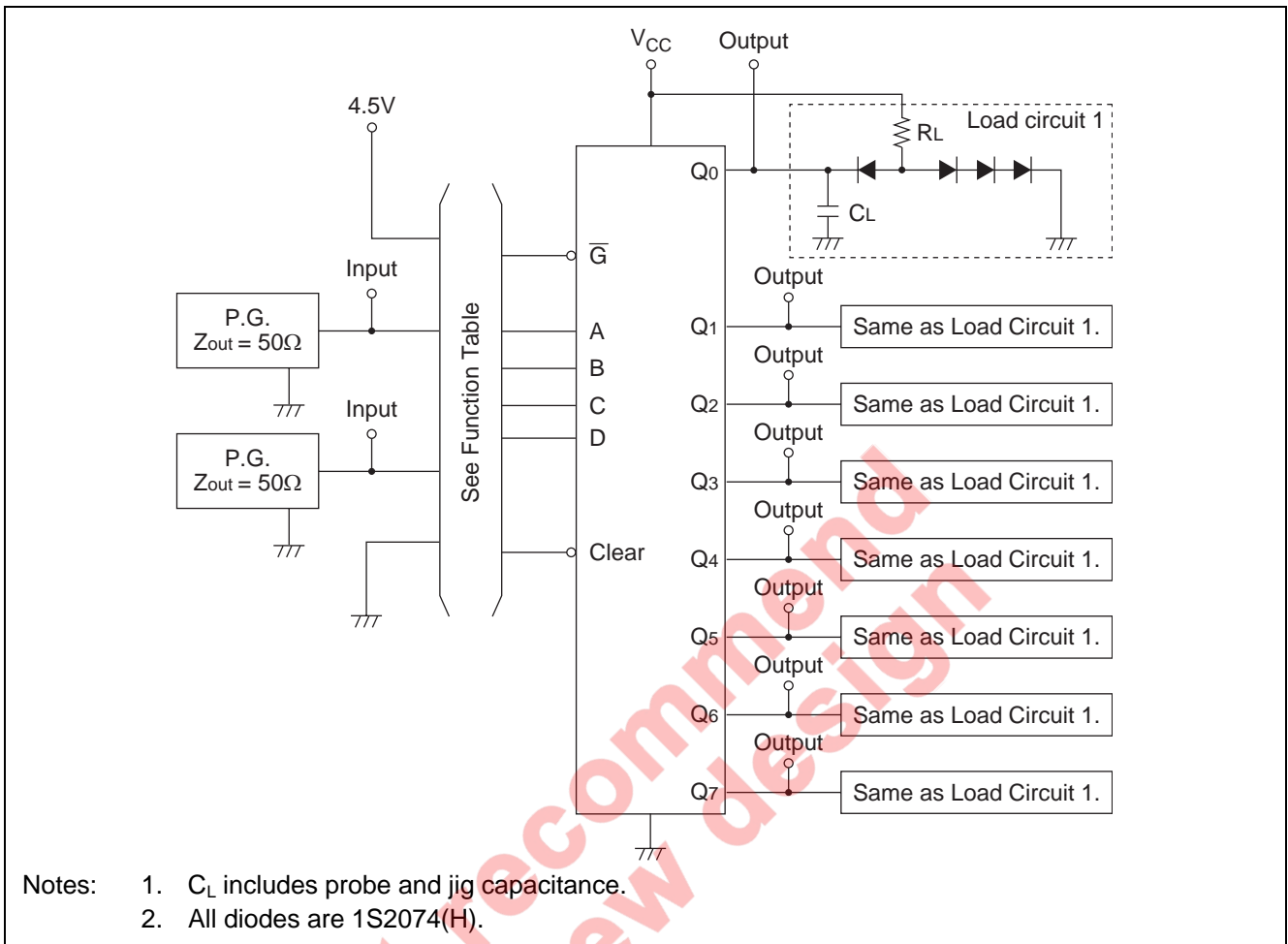
## Switching Characteristics

(V<sub>CC</sub> = 5 V, Ta = 25°C)

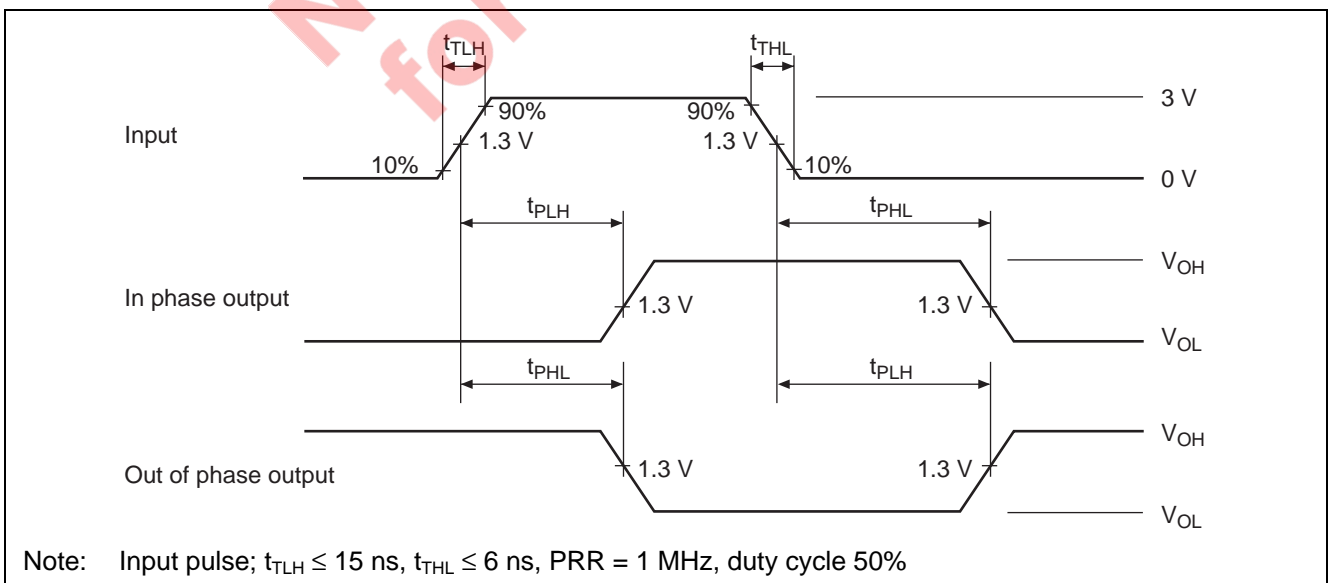
Item	Symbol	Inputs	Output	min.	typ.	max.	Unit	Condition
Propagation delay time	t <sub>PHL</sub>	Clear	Q <sub>0</sub> to Q <sub>7</sub>	—	17	27	ns	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ
	t <sub>PLH</sub>	Data	Q <sub>0</sub> to Q <sub>7</sub>	—	20	32	ns	
	t <sub>PHL</sub>			—	13	21		
	t <sub>PLH</sub>	Address	Q <sub>0</sub> to Q <sub>7</sub>	—	24	38	ns	
	t <sub>PHL</sub>			—	18	29		
	t <sub>PLH</sub>	Enable	Q <sub>0</sub> to Q <sub>7</sub>	—	22	35	ns	
	t <sub>PHL</sub>			—	15	24		

## Testing Method

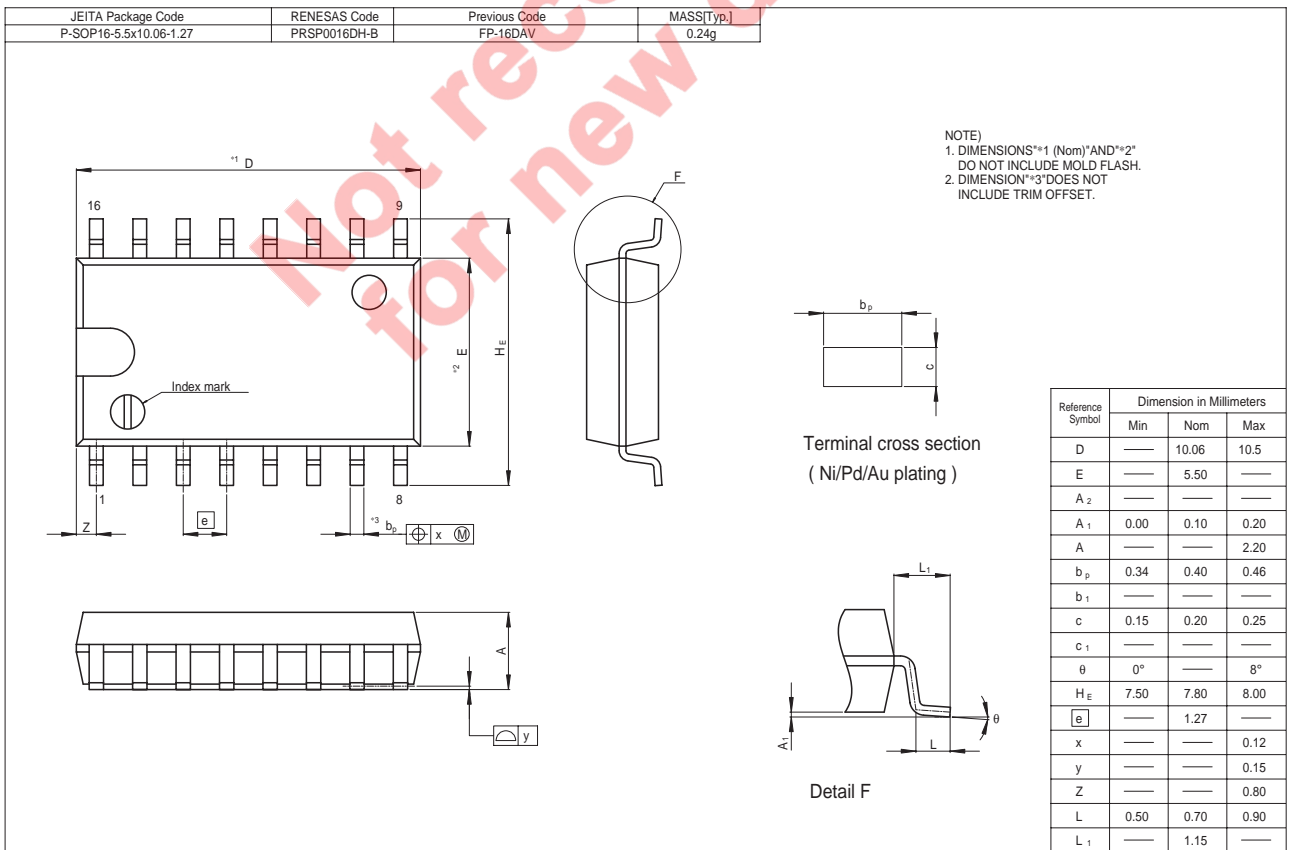
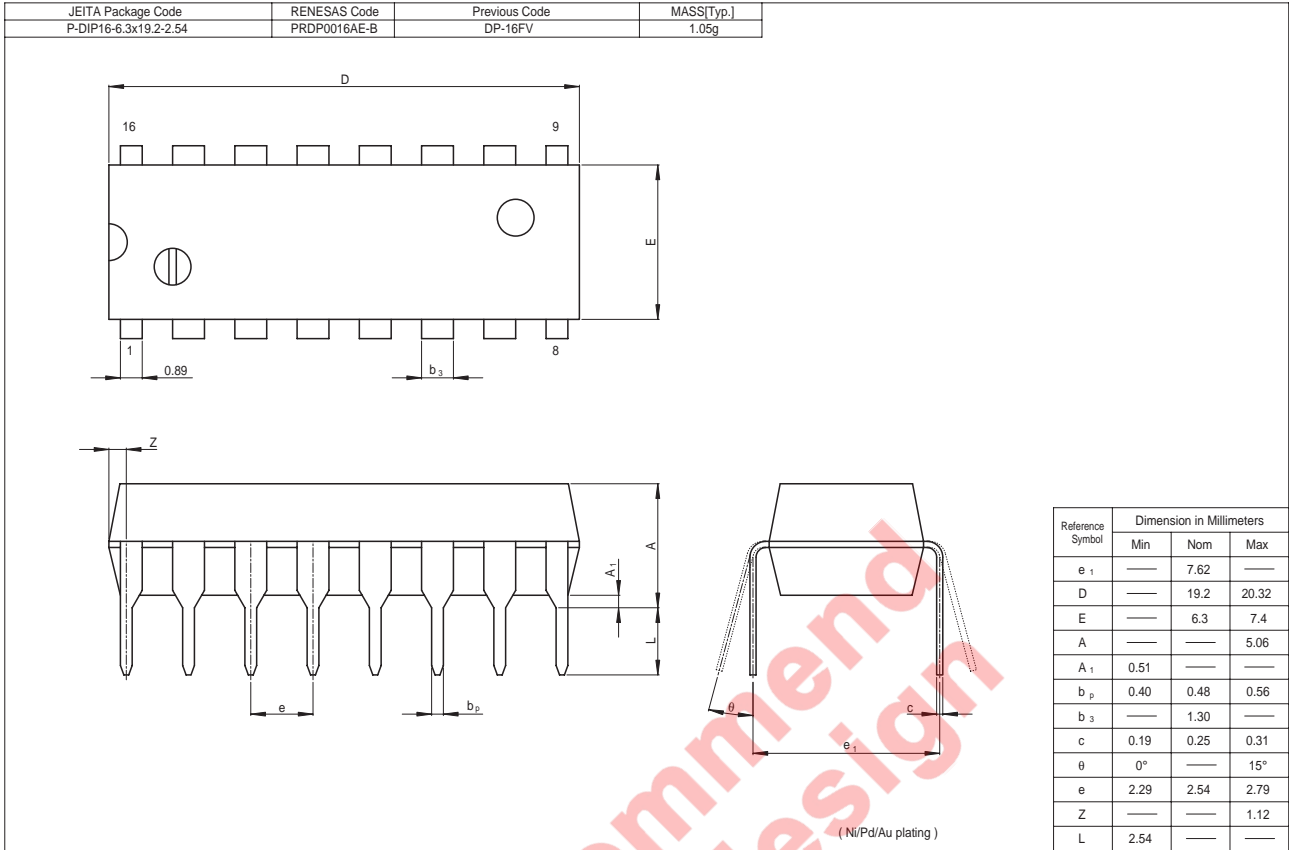
### Test Circuit

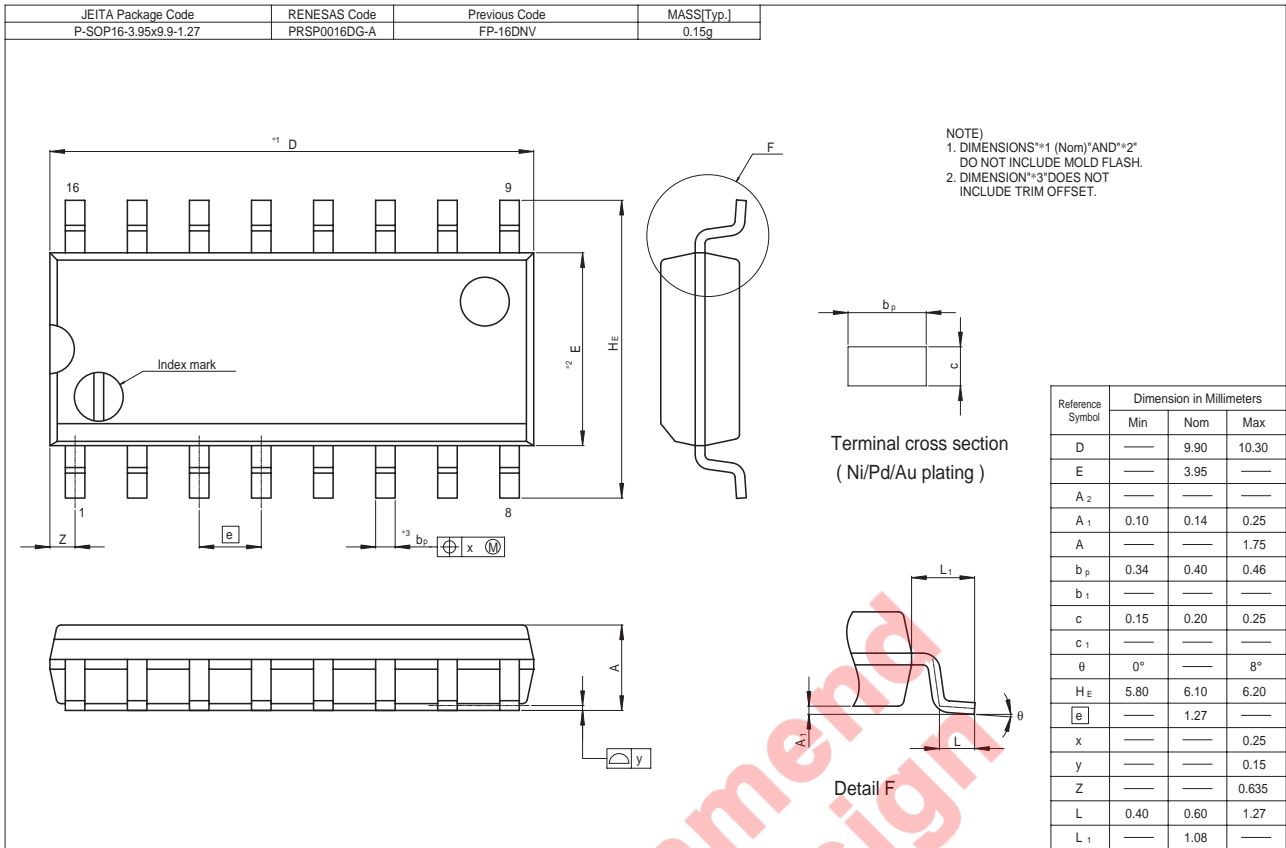


### Waveform



Package Dimensions





Not recommended for new design

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